

Remarks/Arguments:

Reconsideration of the application is requested.

Claims 1-10 and 15 remain in the application. Claim 15 has been amended. Claims 1-10 have been withdrawn. Claims 11-14 and 16-17 have been cancelled.

In item 9 on pages 3-4 of the above-mentioned Office action, claim 15 has been rejected as being unpatentable over Yamagishi et al. (Japanese Patent Application JP 6-291239) in view of Komata et al. (Japanese Patent Application JP 2-15897) and Bacon et al. (US Pat. No. 5,234,153) under 35 U.S.C. § 103(a).

The rejection has been noted and claim 1 has been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on page 1, lines 13 and 17, page 3, lines 17 and 23, and page 6, line 17 of the specification as well as Figs. 2A and 2B.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 15 calls for, inter alia:

a semiconductor chip secured to said substrate by one of alloying and brazing using said solder to form a direct chip-substrate connection. (Emphasis added.)

Yamagishi et al. do not disclose a chip-substrate connection because in Yamagishi et al. there is a further component in the form of a housing between the chip and substrate. The invention of the instant application, therefore, saves a component.

As already discussed in the previous responses, Yamagishi et al. disclose a gold-tin soldered joint between the housing 5 and the substrate 1 and between a lead pin 2 and a pin bearing pad 3. However, there is no chip-substrate connection between the chip 4 and the substrate 1 (see Fig. 1 (C) of Yamagishi et al.).

Komata et al. disclose a method for producing a gold-tin alloy. However, Komata et al. have nothing to do with a semiconductor chip secured to a substrate by using solder and thus forming a chip-substrate connection.

Bacon et al. disclose a permanent metallic bonding method for bonding a laser device to a diamond submount. However, Bacon et al. do not disclose a chip-substrate connection as recited in claim 15 of the instant application.

Clearly, none of the cited references shows "a semiconductor chip secured to said substrate by one of alloying and brazing using said solder to form a direct chip-substrate connection", as recited in claim 15 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 15. Claim 15 is, therefore, believed to be patentable over the art.

In item 10 on pages 4-5 of the above-mentioned Office action, claim 15 has been rejected as being unpatentable over Yamagishi et al. in view of Ishii (Japanese Patent Application JP 6-326210) and Bacon et al. under 35 U.S.C. § 103(a).

As discussed above, Yamagishi et al. and Bacon et al. do not disclose a chip-substrate connection. Ishii discloses a submount interposed between a laser chip 1 and a metal block 5. As can be clearly seen from the drawings of Ishii, the chip 1 and the substrate 10 do not form a chip-substrate connection. Rather, there are a barrier layer 7a and a solder layer 8 between the chip 1 and the substrate 10.

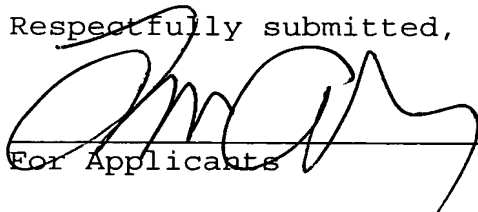
It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 15. Claim 15 is, therefore, believed to be patentable over the art.

In view of the foregoing, reconsideration and allowance of claim 15 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,


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September 26, 2003

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